IN THE CLAIMS:

Please amend claims 1 and 5 as follows:

1. (Currently Amended) A liquid crystal display device having a liquid crystal display panel, a plurality of cascade-connected liquid crystal drive circuits for sequentially transferring a signal, and a plurality of signal lines formed over an edge portion of the liquid crystal display panel for transmitting a signal between any two of the drive circuits, wherein each of the liquid crystal drive circuits comprises:

an image input terminal connected with one of the signal lines to receive an image signal being input thereto;

a clock input terminal connected with another one of the signal lines to receive an external clock signal being input thereto;

a clock compensation circuit for generating an internal clock signal based on the external clock signal thereby compensating for a duty ratio deviation of the external clock signal, said internal clock signal swinging from a first voltage to a second voltage lower than the first voltage;

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a data storage circuit for storing therein the image signal at a timing of a voltage change from the first voltage to the second voltage or at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal;

a data bus for transmitting the image signal from the data storage circuit;

a voltage select circuit for selecting a voltage for driving the liquid display panel; and

a clock signal output circuit for outputting the internal clock signal as a subsequent external clock signal to a subsequent liquid crystal drive circuit, said clock signal output circuit having a delay circuit,

wherein the delay circuit delays the internal clock signal to become the subsequent external clock signal to the subsequent liquid crystal drive circuit so as to provide phase margins thereof in a dual-edge accept scheme.

2. (Original) The liquid crystal display device as claimed in Claim 1, wherein the clock compensation circuit has a phase locked loop circuit.

3. (Original) The liquid crystal display device as claimed in Claim 1, wherein the clock compensation circuit has a delay locked loop circuit.

4. (Original) The liquid crystal display device as claimed in Claim 1, wherein the data bus comprises two systems of signal lines.

5. (Currently Amended) A liquid crystal display device having a liquid crystal display element, a plurality of cascade-connected liquid crystal drive circuits, and a plurality of signal lines formed over an edge portion of the liquid crystal display ~~panel~~ element for transmitting a signal between any two of the drive circuits, wherein each of the liquid crystal drive circuits comprises:

a data input terminal connected with one of the signal lines to receive an image signal being input thereto;

a clock compensation circuit for inputting an external clock signal and outputting an internal clock signal, the internal clock signal having a first period for outputting a first voltage and a second period for outputting a second voltage;

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a data latch circuit for taking thereto the image signal at a timing of a voltage change from the first voltage to the second voltage or at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal;

a data bus for transmitting the image signal from the data latch circuit;

a voltage output circuit for outputting a voltage selected according to the image signal on the data bus to the liquid crystal display element;

a data output circuit for outputting the image signal on the data bus to a subsequent liquid crystal drive circuit;

a clock formation circuit being operable to correct a duty ratio deviation ~~from~~ of the external clock signal to provide the internal clock signal; and

a clock signal output circuit for outputting the internal clock signal as a subsequent external clock signal to a subsequent liquid crystal drive circuit, said clock signal output circuit having a delay circuit,

wherein the internal clock signal is delayed to become the subsequent external clock signal by the delay circuit so as to provide phase margins thereof in a dual-edge accept scheme.

6. (Original) The liquid crystal display device as claimed in Claim 5, wherein the clock formation circuit has a phase locked loop circuit.

7. (Original) The liquid crystal display device as claimed in Claim 5, wherein the clock formation circuit has a delay locked loop circuit.

8. (Original) The liquid crystal display device as claimed in Claim 5, wherein the data bus comprises tow systems of signal lines.

9. (Previously Presented) The liquid crystal display device as claimed in Claim 1, wherein the duty ratio deviation of the external clock signal is caused by at least one of an internal characteristic of the respective drive circuit and a factor on the signal lines.

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10. (Previously Presented) The liquid crystal display device as claimed in Claim 1, wherein the internal clock signal generated by the clock compensation circuit has a duty ratio of 50%.

11. (Previously Presented) The liquid crystal display device as claimed in Claim 5, wherein the duty ratio deviation of the external clock signal is caused by at least one of an internal characteristic of the respective drive circuit and a factor on the signal lines.

12. (Previously Presented) The liquid crystal display device as claimed in Claim 5, wherein the internal clock signal generated by the clock compensation circuit has a duty ratio of 50%.

13. (Original) The liquid crystal display device as claimed in Claim 1, wherein the clock compensation circuit has an inverter.

14. (Original) The liquid crystal display device as claimed in Claim 5, wherein the clock formation circuit has an inverter.

15. (Original) The liquid crystal display device as claimed in Claim 1, wherein the voltage select circuit selects the voltage according to the image signal on the data bus and then outputting the selected voltage.

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